### **2014 DOE VEHICLE TECHNOLOGIES ANNUAL MERIT REVIEW**

Next Generation Inverter

Project ID # EDT040



Presenter: Zilai Zhao **General Motors** June 10, 2015























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This presentation does not contain any proprietary, confidential, or otherwise restricted information.

### **OVERVIEW**

### **Timeline**

- Start October 2011
- Finish January 2016
- 85% Complete

### **Barriers**

- Cost
- Efficiency
- Performance and Lifetime
- Mass and Volume

### **Funding**

	DOE	GM
Budget	\$6.0M	\$10.6M
FY12	\$0.80M	\$1.97M
FY13	\$1.70M	\$3.43M
FY14	\$1.80M	\$3.31M
FY15 (thru March)	\$0.30M	\$0.91M
Actual (thru Mar-15)	\$4.60M	\$9.32M

### **Partners**

- Lead General Motors
- Tier 1, 2, & 3 Suppliers Hitachi, Delphi, Infineon, HRL,
  Panasonic, AVX, Kemet, and
  VePoint
- Collaborations National Renewable Energy Laboratory, and Oak Ridge National Laboratory

### **RELEVANCE**

#### Research Focus Area: Inverter

- Modularity/Scalability
- Components power module, gate drive, capacitor, current sensor and control card
- Supplier development

### Objective

 Develop the technologies and product design for a low cost highly efficient next generation inverter capable of 55kW peak/30kW continuous power.

### Addresses Targets

- Cost: \$3.30/kW produced in quantities of 100,000 units
- Power Density: 13.4kW/l; Specific power: 14.1kW/kg
- Efficiency >94% (10%-100% speed at 20% rated torque)

### Uniqueness and Impacts

- Technology Co-development with the Tier 1, 2, and 3 suppliers
- Detailed knowledge of vehicle application and ability to understand and assess vehicle impacts to make necessary materials and technology tradeoffs.

### **MILESTONES**

Month /Year	Milestone or Go/No-Go Decision	Status
June 2012	Power Inverters Based on Conventional, Transfer Molded, and Encapsulated Power Module Technology Delivered for Evaluation	Complete
Jan 2013	Initial Technology and Production Cost Assessment Complete with Report	Complete
Jan 2014	Concept Design Review – DOE "Go/No-Go" Decision	Complete
Sept. 2014	Critical Design Review (original scheduled for June 2014)	Complete
Aug. 2015	Demonstration of Inverter Performance	On track
Sept. 2015	Final cost estimation (originally scheduled for Sept. 2014)	On track
Dec. 2015	Preliminary reliability study	On track

### **ACCOMPLISHMENT: HIGH POWER DENSITY**

# of 3ph bridges
kVA/L
kVA/kg

SPIM1	SPIM2	NGI Lo/Hi
1	1	1
14.6	21.8	31.4 / 38.7
14.6	22.7	24.4 / 30.0

TPIM1	TPIM2	TPIM3
2	2	2
34.6	23.7	26.8
25.5	26.7	23.9

#### Note

- DOE's 2020 targets for a 55 kW single inverter are 13.4kW/L and 14.1kW/kg.
- Dual inverters have higher power density due to sharing of components between the two 3-phase bridges.
- Manufacturability vs. Volume tradeoff: High power density could lead to high cost
- Next Gen Inverter pushes for even higher volumetric power density
  - Smaller: Easier to package in vehicle
  - Smaller: Less materials and less expensive
  - Inverter level optimization: all components must be optimized for the chosen inverter architecture
  - Manufacturability must be improved simultaneously

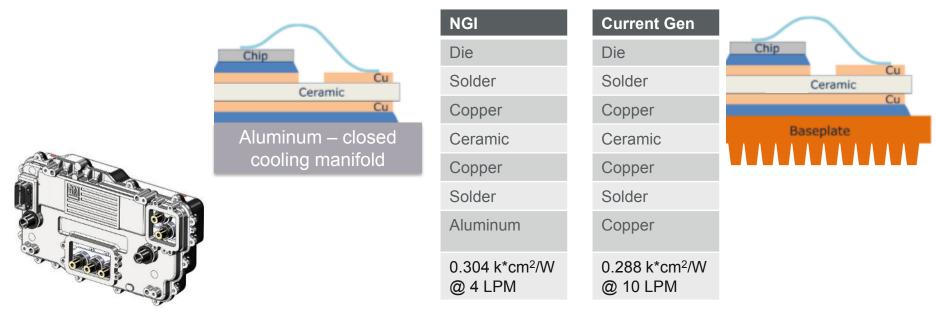


### KEY ACCOMPLISHMENT: INTEGRATED POWER STAGE



- Integrated power stage: Eliminate boundaries and empty spaces; new partitioning of functionality
- Vertically integrated process: Power stage manufacturing integrated into inverter assembly
- Manufacturability: Unidirectional (bottom to top) assembly process; reduced assembly steps

### KEY ACCOMPLISHMENT: DBC DIRECTLY ATTACHED TO CLOSED COOLING MANIFOLD

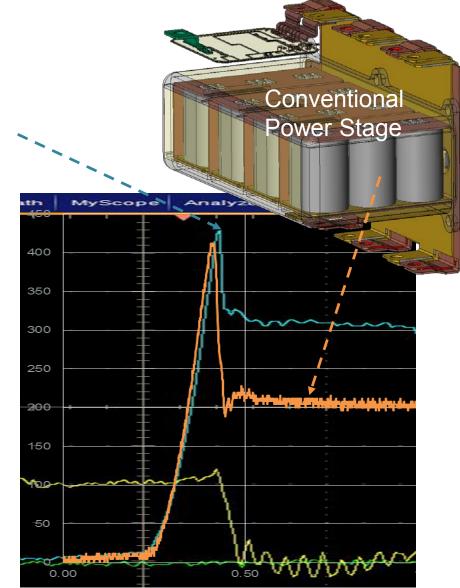


- Switching circuitry built directly on closed cooling manifold
- Thermal performance on par with Cu pin-fin base-plate
- Manufacturability
  - DBC to Al attach is a challenge
  - Vertically integrated process

# KEY ACCOMPLISHMENT: LOW INDUCTANCE DC LOOP (INVERTER LEVEL)



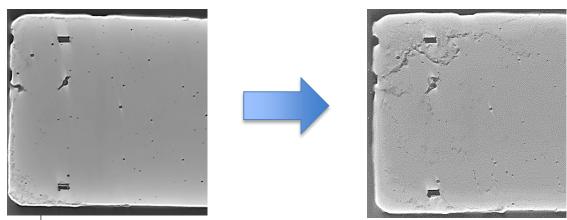
- Low stray inductance in the complete DC loop
- Manufacturability
  - Vertically integrated process
  - Press-fit pins



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### **KEY ACCOMPLISHMENT: PROCESS DEVELOPMENT**

- Key Processes: die attach, DBC attach, wire bonding, encapsulation of dies and cap bobbins, press-fit pin, final assembly
- Die/DBC attach
  - 20+ configurations evaluated oven type, solder type, processing parameters
  - Evaluation: Yield, thermal shock (-55°C to 150°C), 3D Xray, Cross-Sectioning
- Encapsulation
  - 5 Configurations evaluated chemistry, process parameters
  - Evaluation: High temp / high humidity



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3D X-Ray: DBC attach before and after thermal shock

### **ACCOMPLISHMENT: PROCESS FLOW**

Substrate Asm

Manifold Asm

Attach

Clean / X-ray / Insp.

**Press Coolant Fittings** 

Press Cap to Pwr Plane

Fab / Test Ctrl/GD Brd

Clean Ctrl/GD Brd

Prep cast frame

Frame Asm & Fast.

Interconnect

**Cure Adhesive** 

**Electrical Test** 

Feed Thru / I-Sen / Fast

Press Power Plane Asm

Silgard / Degas / Cure

Cap potting / Cure

Spacer Frame

Press Control Board & Fast

Harness & Cover

**EOL Test** 

Adhesive Disp.







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### **NEXT STEPS AND FUTURE WORK**

- Finish asset builds
- Complete tests per plan and reliability analysis
- Performance demonstration
- Final cost assessment
- Scalability and further process improvement for WBG devices

### **SUMMARY**

- Inverter level optimization is necessary to achieve high power density with reasonable manufacturability.
- Integrated power stage design and vertically integrated process can lead to desired targets.
- DOE's funding helps GM design and build prototypes to show/achieve the potential of inverter level optimization.

### THANK YOU FOR YOUR ATTENTION!

















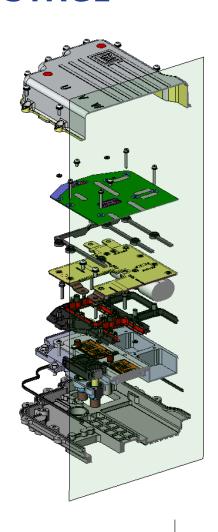




### **TECHNICAL BACKUP SLIDES**

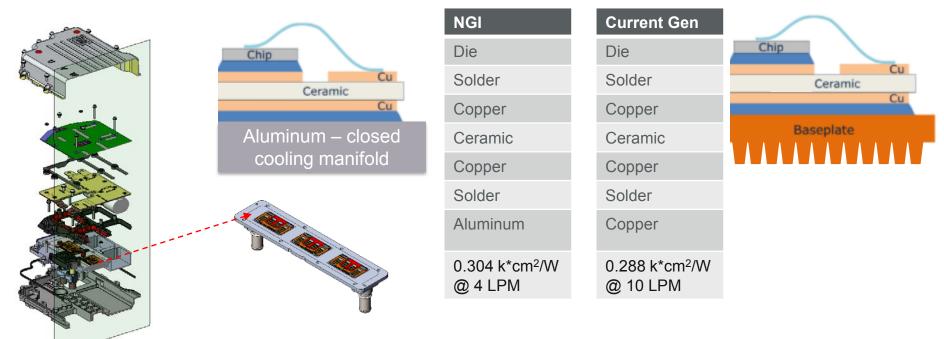


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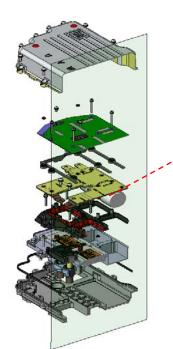
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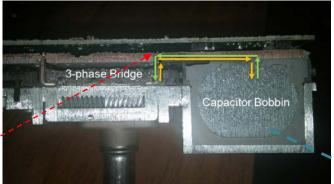
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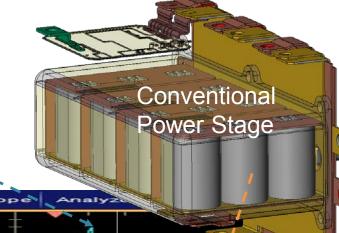


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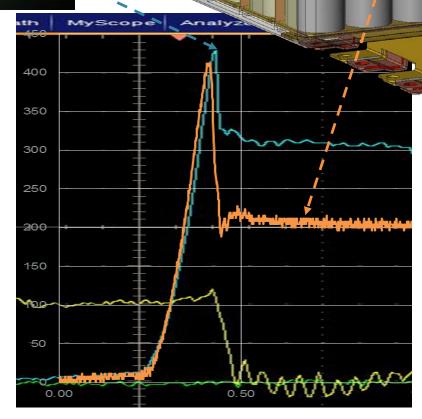
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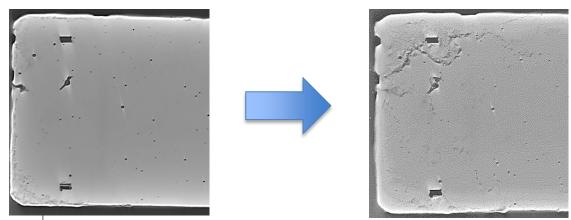
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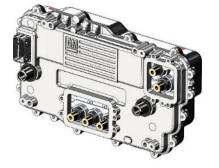
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**Next Steps**